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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,608	02/23/2004	Peter Ramyalal Suaris	1011-67730	3195

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KLARQUIST SPARKMAN, LLP
121 SW SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,608	SUARIS ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) *14-65* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/13/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Group I, claims 1-13 in the reply filed on November 13, 2006 is acknowledged. The traversal is on the ground(s) that the search and/or examination can be made without serious burden. This is not found persuasive because the claimed groups of different methods (species of) re-implementing memory modules would require different searches.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fung (US Patent Application Publication 2005/0204325) in view of Wallace (US Patent Application Publication 2006/0117280).

3. As for the claims, Fung discloses the invention substantially as claimed, including:

1. A method of re-implementing at least one memory module having an undesirable timing delay, the at least one memory module being on an FPGA device, the FPGA device comprising generic logic blocks and dedicated logic blocks, the at least one

memory module being implemented by a first set of at least one of the logic blocks, the at least one logic block of said first set has at least one critical pin, the method comprising:_

(a) identifying the at least one memory module [abstract];

(b) selecting a second set of logic blocks for use in re-implementing said at least one memory module, at least a first logic block of the said second set having, the first logic block of the second set being non-identical

to the at least one logic block of the first set [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048]; and

(c) selectively re-implementing the at least one memory module using the second set of logic blocks in the event that re-implementation using the second set of logic blocks reduces the undesirable timing delay of the at least one memory module [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048];

2. A method according to claim 1 wherein the second set comprises at least one dedicated memory logic block and at least one generic logic block [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element];

3. A method according to claim 1 wherein the first set comprises only generic logic blocks and the second set comprises at least one dedicated memory logic block [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the implemented and re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element];

4. A method according to claim 1 wherein the first set comprises at least one dedicated memory logic block and the second set comprises at least one more dedicated memory logic block than the said first set [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the implemented and re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element];

5. A method according to claim 1 wherein the first set comprises at least one dedicated

memory logic block and the second set comprises only generic logic blocks [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the implemented and re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element];

6. A method according to claim 1 wherein the act of identifying the at least one memory module comprises performing physical timing analysis on at least said one memory module, the method further comprising performing physical timing analysis on said at least one memory module, and wherein the method further comprises performing physical timing analysis on the re-implemented memory module using the second set of logic blocks prior to selecting the re-implementation of the at least one memory module using the second set of logic blocks [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the implemented and re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element; paragraphs 0046 – physical timing analysis, 0048, 0052 – meaning that during the iterative process, Fung may reverse decisions or may come early to irreversible (or correct) decisions];

7. A method according to claim 1 comprising the act of reversing the re-implementation to an implementation of the at least one memory module using the first set of logic blocks in the event the undesirable timing delay of the at least one memory module is not sufficiently reduced upon re-implementation using the second set of logic blocks [paragraphs 0048, 0052 – meaning that during the iterative process, Fung may reverse decisions or may come early to irreversible (or correct) decisions];

8. A method according to claim 1 comprising repeating the acts of claim 1 for one or more additional sets of logic blocks which are non-identical to one another and which are non-identical to the first and second sets [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element – further Fung's process is iterative or updated];

9. A method according to claim 8 in which the selectively re-implementing act

comprises the act of selecting a set of logic blocks for re-implementing the at least one memory module which eliminates the undesirable timing delay [paragraphs 0009-0010, 0013-0018, 0022, 0038, 0046, and 0048 – especially paragraph 0038 where the re-implemented logic blocks may be of any nature, including memory blocks as well as any other logic element];

10. A method according to claim 8 comprising the act of reversing a subsequent re-implementation of the at least one memory module to a prior implementation or prior re-implementation in the event the undesirable timing delay of the at least one memory module is not sufficiently reduced by the subsequent re-implementation of the at least one memory module [paragraphs 0046 – physical timing analysis, 0048, 0052 – meaning that during the iterative process, Fung may reverse decisions or may come early to irreversible (or correct) decisions];

11. A computer programmed to implement the method of claim 1 [paragraph 0137-0138];

12. Computer readable media programmed with computer readable instructions to carry out the method of claim 1 [paragraph 0137-0138];

13. For use in a computer system, a design database of FPGA programming instructions stored on computer readable media for a re-implemented memory module which has been re-implemented in accordance with the method of claim 1 [paragraph 0137-0138];

Fung does not specifically disclose that the logic block of the second set has a pin that is logically equivalent to said at least one critical pin of the at least one logic block of said first set or performing the physical timing analysis to identify the at least one critical pin of said first set of at least one logic block.

Wallace discloses swapping circuits with equivalent pins and identifying critical pins [paragraphs 0028, 0033, 0035, 0037-0039].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Fung and Wallace because utilizing re-implemented logic with equivalent pins or performing physical timing analysis for pin criticality within Fung's system would have improved Fung's design by providing a fix for timing problems by switching to faster pins of re-implemented logic blocks [see Wallace, especially paragraph 0038].

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
November 22, 2006